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17. (currently amended) A method of fabricating a multi-bit flash memory, comprising:

providing a substrate;

forming a tunneling oxide layer on the substrate;

forming a germanium polycide layer on the tunneling oxide layer;

forming a patterned photoreist layer on the germanium polycide layer, the patterned photoresist layer exposing a part of the germanium polycide layer predetermined for forming an isolation region;

performing an ion implantation step to implant dopant into the exposed germanium polycide layer;

performing an annealing process to react the dopant with silicon of the germanium polycide layer to form ~~the~~ an isolation region that partitions the germanium polycide into ~~a plurality of~~ more than two conductive blocks arranged in an array, the array having a plurality of rows extending from a region predetermined for forming a bit line to a region predetermined for forming another bit line and a plurality of columns each having said ~~n~~ ~~(n is a positive integer)~~ conductive blocks;

forming a gate dielectric layer on the germanium polycide layer;

patterning the gate dielectric layer and the germanium polycide layer to form a floating gate;

forming the bit lines in the substrate at two sides of the floating gate;

forming a control gate on the floating gate; and

performing a step of threshold voltage adjustment to result in different threshold

voltages of the channel regions under the conductive blocks of different rows.

18. (original) The method according to Claim 17, wherein the step of ion implantation further comprises implanting oxygen ions into the exposed germanium polycide layer.

19. (original) The method according to Claim 17, wherein the step of ion implantation further comprises implanting nitrogen ions into the exposed germanium polycide layer.

20. (original) The method according to Claim 17, further comprising forming a field oxide and a spacer on a sidewall of the floating gate after the step of forming the bit lines and before the step of forming the control gate.

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CONCLUSION

Pursuant to Examiner's instruction, a complete listing of all the claims is now presented. If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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